WHAT IS CLAIMED IS:

1. A computer system comprising:

a host processor;

a plurality of memory devices;

an interface interposed between the host processor and the plurality of memory devices, wherein the interface comprises:

a data control register comprising a plurality of select bits corresponding to the plurality of memory devices, and such that write access to a specific one of the plurality of memory devices is enabled if a corresponding one of the plurality of select bits is set; and

a control register comprising a plurality of control bits corresponding to the plurality of memory devices, wherein the state of the control bits are set by the host processor to enable the control bits to be copied to the select bits.

2. The system as recited in claim 1, wherein the host processor enables write access to any combination of the plurality of memory devices by setting the corresponding control bits and then copying the control bits to the select bits.

3. The system as recited in claim 2, wherein, after enabling write access to the combination of memory devices, the host processor writes data simultaneously to the entire combination of write enabled memory devices.

4. The system as recited in claim 3, wherein each of the plurality of memory devices comprises both an instruction memory device and a data memory device, and wherein an extended memory bit in the control register selects either instruction memory devices or the data memory devices to be write enabled when the corresponding data control bits are set.

5. The system as recited in claim 4, further comprising a plurality of secondary processors such that a specific one of the plurality of instruction memory devices and a specific one of the plurality of data memory devices is coupled to each of the plurality of secondary processors.

6. The system as recited in claim 5, wherein the host processor is adapted to load the instruction memory coupled to any of the plurality of secondary processors with program instructions executable by said secondary processor.

7. The system as recited in claim 1, wherein a write enable bit within the control register enables the copying of the control bits to the select bits.

8. The system as recited in claim 1, further comprising peripheral devices, including serial ports and a direct memory access controller, operatively coupled to each of the plurality of secondary processors.

9. The system as recited in claim 8, wherein the host processor interface and the secondary processors, together with their associated memory devices and peripheral devices, all share a monolithic semiconductor substrate.

10. The system as recited in claim 1, wherein the secondary processors are digital signal processors.

11. The system as recited in claim 1, wherein the interface further comprises an instruction decoder, such that setting the state of the control bits and copying of the control bits to the select bits occur when the instruction decoder responds to a command issued by the host processor to the interface.

12. The system as recited in claim 11, wherein the command is issued solely by the host processor absent any commands issued by the interface.

13. A method for distributing data to a plurality of memory devices, the method comprising:

placing data on a data bus coupled to the plurality of memory devices;

setting at least one of a plurality of control bits within a control register, wherein each of the control bits corresponds to a specific one of the plurality of memory devices;

copying the control bits to corresponding select bits in a data control register;

activating write enable signals to the memory devices for which the corresponding control bits are set; and

writing the data to those memory devices whose write enable signals are active.

14. The method as recited in claim 13, wherein the data is distributed to the memory devices by a host processor and each of the memory devices is coupled to a specific one of a plurality of secondary processors.

15. The method as recited in claim 14, wherein both an instruction memory device and a data memory device are coupled to each of the plurality of secondary processors, and wherein the method further comprises using an extended memory bit in the control register to activate the write enable signals for either the instruction memory devices or the data memory devices.

16. The method as recited in claim 13, wherein both the control register and the data control register are contained within an interface interposed between the host processor and the memory devices.

17. The method as recited in claim 16, further comprising the interface decoding commands from the host processor.

18. The method as recited in claim 17, further comprising the interface responding to a specific command by copying the control bits to the select bits, without intervention by the host processor.

19. The method as recited in claim 18, further comprising distributing to the instruction memory coupled to any of the plurality of secondary processors program instructions executable by said secondary processor.

20. A memory medium, comprising:

a first set of bits corresponding to a set of memory devices;

a second set of bits which are operable to set a corresponding set of write enable lines coupled to a respective set of memory devices; and

means for operating the second set of bits solely from a host processor link coupled to but external from a monolithic substrate containing the set of memory devices.

21. The memory medium as recited in claim 20, wherein the first and second sets of bits are contained within a control register and a data control register configured within the monolithic substrate.